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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,791	11/03/2003	Ernest Allen III	03-0724/LSI1P230	5486

7590 03/21/2005

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,791	ALLEN ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-9,13-17 and 19* is/are rejected.

7)☒ Claim(s) *5,6,10-12,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: in line 4 of the claim, the limitation "the functional relationship" should be changed to --a functional relationship-- in order to avoid an insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 8-9, 13-14 and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kalb, Jr. (5742177).

Regarding claim 1, Kalb, Jr. discloses a method for testing a semiconductor device [see Abstract], the method comprising: measuring [see steps 410 and 420 in Fig. 4] for a first semiconductor device a first current (IDDQ1) at a first voltage (V1) and a second current (IDDQ2) at a second Voltage (V2) [see col. 6, lines 13-18]; identifying the functional relationship (temperature and/or voltage) between the first (IDDQ1) and second currents (IDDQ2); and comparing [see steps 440-442] the functional relationship (temperature and/or voltage) to a predetermined relationship to determine whether the device is defective [see col. 6, lines 19-23].

Regarding claim 2, Kalb, Jr. discloses the functional relationship (temperature and/or voltage) is a ratio between the first and second currents [see col. 4, line 52-col. 6, line 11].

Regarding claims 3-4, Kalb, Jr. discloses the first semiconductor device is a transistor or an integrated circuit.

Regarding claim 8, Kalb, Jr. discloses the first (IDDQ1) and second (IDDQ2) currents are quiescent currents [see col. 6, lines 13-18].

Regarding claim 9, Kalb, Jr. discloses the device is determined [see steps 440-442] to be defective if it deviates from the predetermined relationship by a predetermined threshold [see col. 6, lines 24-34].

Regarding claims 13-14, Kalb, Jr. discloses the first (IDDQ1) and second (IDDQ2) currents are supplied and measured by automated test equipment [not shown].

Regarding claim 16, Kalb, Jr. discloses a method for testing a semiconductor die [see Abstract], the method comprising: measuring [see steps 410 and 420] for the semiconductor die at least two quiescent currents (IDDQ1 and IDDQ2), the first current (IDDQ1) of the two quiescent currents measured when a first supply voltage (V1) is applied to a supply terminal of the die and the second current (IDDQ2) measured when a second supply voltage (V2) is applied to the supply terminal of the die; determining [step 430] a measured ratio between the first (IDDQ1) and second currents (IDDQ2); comparing [see steps 440-442] the measured ratio with an expected ratio for quiescent currents (IDDQ1 and IDDQ2); and determining if the die is defective when the measured ratio differs from the expected ratio by a predetermined threshold [see col. 6, lines 24-34].

Regarding claim 17, Kalb, Jr. discloses the first (IDDQ1) and second (IDDQ2) currents are measured by automated test equipment [not shown].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalb, Jr. (5742177) in view of Miller (6239606).

Regarding claims 7 and 19, Kalb, Jr. discloses a method for testing a semiconductor device [see Abstract], the method comprising: measuring [see steps 410 and 420 in Fig. 4] for a first semiconductor device a first current (IDDQ1) at a first voltage (V1) and a second current (IDDQ2) at a second Voltage (V2) [see col. 6, lines 13-18]; identifying the functional relationship (temperature and/or voltage) between the first (IDDQ1) and second currents (IDDQ2); and comparing [see steps 440-442] the functional relationship (temperature and/or

voltage) to a predetermined relationship to determine whether the device is defective [see col. 6, lines 19-23]. However, he does not disclose measuring a third current at a third voltage as claimed. Miller disclose a method for testing a semiconductor device [see Abstract], the method comprising: measuring [see steps 600, 604 and 608 in Fig. 6] for a first semiconductor device a first current (first quiescent current) at a first voltage, a second current (second quiescent current) at a second voltage and a third current (third quiescent current) at a third voltage [see col. 6, lines 3-9]; and comparing [see steps 610] the functional relationship to a predetermined relationship to determine whether the device is defective [see col. 6, lines 12-16]. Further, Miller teaches that the addition of measuring a third current is advantageous because it may be found to fail only those devices wherein a defect is detected two or more times in the event that the first detection was an error or is not repeatable. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Kalb, Jr. by adding a third current measuring as taught by Miller in order to failed only those devices wherein a defect is detected two or more times in the event that the first detection was an error or is not repeatable.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ooshima et al (5321354), Miller (5889408 & 6239605), Kalb, Jr. (5889409 & 6242934), Sugasawara et al (6239609), Okayasu (6590405) and Hachn et al (6623992) disclose a method and apparatus for inspecting a semiconductor devices.

8. Claims 5-6, 10-12, 15 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 5, the primary reason for the allowance of the claim is due to method for testing a semiconductor device comprising the predetermined relationship is determined by evaluating the functional relationship for at least one other die on the same wafer.

Regarding claim 6 the primary reason for the allowance of the claim is due to method for testing a semiconductor device comprising the predetermined relationship is determined from a plurality of dies fabricated previously.

Regarding claim 10, the primary reason for the allowance of the claim is due to method for testing a semiconductor device comprising the functional relationship is a ratio of the first and second currents and the predetermined threshold is about 20 % of the value determined for the ratio.

Regarding claim 11, the primary reason for the allowance of the claim is due to method for testing a semiconductor device comprising the first and second voltages are set within the range from 50 to 140 % of a nominal supply voltage for the device.

Regarding claim 12, the primary reason for the allowance of the claim is due to method for testing a semiconductor device comprising the first and second voltages are set within the range from 60 to 120 % of a nominal supply voltage for the device.

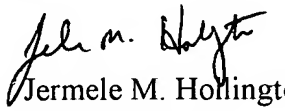
Regarding claim15, the primary reason for the allowance of the claim is due to method for testing a semiconductor device comprising the predetermined relationship comprises a running average of the functional relationship for the devices previously tested.

Regarding claim 18, the primary reason for the allowance of the claim is due to method for testing a semiconductor device comprising the first and second voltages are set within the range from 50 to 140 % of a nominal supply voltage for the device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
March 15, 2005